Amendments to the Specification

Please replace the paragraph beginning at page 2, line 6 with the following rewritten paragraph:

-- For a more complete understanding of the invention, FIG. 1 illustrates a circuit model diagram of a conventional output buffer 10 of an integrated circuit. Output driver 10 generally includes a pullup transistor 12 (such as p-channel field effect transistor (PFET) P1) and a pulldown transistor 14 (such as n-channel field effect transistor (NFET) N1). Output driver 10 also generally includes a predriver circuit 6 which generates a pullup signal PULLUP to control the pullup transistor 12 and a pulldown signal PULLDOWN to control the pulldown transistor 14. Predriver circuit 6 determines the states of pullup signal PULLUP and pulldown signal PULLDOWN based on the state of received data signal DATA, and typically also on the state of an output enable signal OE. Output enable signal OE is used to place the driver 10 into a high-impedance state whereby the driver 10 does not actively drive the pad 8. When the output driver 10 is enabled to actively drive the pad 8, the output signal OUT to be driven onto the pad 8 is derived from the data signal DATA, and is characterized by a driver output impedance Z_D.--

Please replace the paragraph beginning at page 8, line 18 with the following rewritten paragraph:

-- As known in the art, the load capacitance and the impedance ~~resistance~~ (parallel combination of output impedance Z_D ~~termination resistance R_O~~ and transmission line characteristic impedance Z_O) add to the RC time constant of the signal, which affects how quickly the output signal transitions. As also known in the art, the voltage on a transmission line rises or falls in accordance with the equation: $V(t) = V_O * e^{-t/RC}$ where V_O is the initial voltage, t is time and RC is the time constant of the RC circuit (i.e., the product of the

impedance (or Thevenin equivalent resistance) and capacitance). In accordance with the invention, since the output impedance Z_D ~~resistance R_O~~ of the driver circuit is known, the chip designer can choose a redistribution metal having a characteristic capacitance C_O (typically determined by the length and width of the redistribution metal) corresponding to a resulting desired slew rate.--

Please replace the paragraph beginning on page 8, line 29 with the following rewritten paragraph:

-- FIG. 3 depicts a method 100 for controlling the slew rate of integrated circuit signals in accordance with the invention. As illustrated, the designer determines (step 102) the output impedance Z_D ~~resistance R_O~~ of the signal driver driving the signal of interest. The output impedance Z_D ~~resistance R_O~~ is determined by the sizes of the transistors implementing the output driver cell.--

Please replace the paragraph beginning at page 9, line 1 with the following rewritten paragraph:

--The capacitance required to produce an RC time constant which will result in a desired slew rate on the transmission line is calculated (step 104), taking into account the output impedance Z_D ~~resistance R_O~~ of the signal driver.--

Please replace the paragraph beginning at page 9, line 4 with the following rewritten paragraph:

-- The designer then selects (step 106) a redistribution metal having a characteristic capacitance C_{RM} which, given the known output impedance Z_D ~~resistance R_O~~ of the signal driver, will produce a desired slew rate for the transitioning edges of the signal driven onto the transmission line. --

Please replace the paragraph beginning at page 9, line 31 with the following rewritten paragraph:

-- Since the output impedance Z_D ~~resistance R_O~~ of the output driver cell 112a is known from the design, the goal is to map the output driver cell 112a to one of the die pads 70a-70h whose proposed connective redistribution metal 115a-115h is characterized by a respective capacitance C_{Ra}-C_{Rh} that will produce an RC time constant appropriate for generating a desired transmission line slew rate for the signal generated by the output driver cell 112a.--

Please replace the paragraph beginning at page 10, line 8 with the following rewritten paragraph:

--FIG. 4D also illustrates the mapping possibilities for output driver cell 112b given the mapping assignment of output driver cell 112a. In this illustration, output driver cell 112b has the possibility of interconnection to any one of the die pads 70a, or 70c-70h. During layout, the characteristic capacitance of the redistribution metal required to connect the output driver cell 112b to each of die pads 70a and 70c-70h is estimated. The output driver cell 112 is mapped to one of the die pads 70a, 70c-70h whose connective redistribution metal is characterized by a capacitance C_R that will produce a desired RC time constant appropriate for generating the desired transmission line slew rate given the known output impedance Z_D ~~resistance R_O~~ of the output driver cell 112b.--

Please replace the paragraph beginning at page 12, line 5 with the following rewritten paragraph:

--The parasitics of each interconnect component to be modeled (e.g., pads, vias, routing metal, bonds) can be predicted during the floorplanning stage. At the floorplanning stage, although the impedance ~~resistance~~ of the various components of the

interconnect path cannot be predicted since the shape of the interconnect is not known until the routing stage, the total length of the interconnect can be estimated and thus the total capacitance estimated. Techniques exist for estimating capacitance as a function of net fanout and block size. A floorplanning tool can then use these predicted-capacitance tables (also known as interconnect-load tables or wire-load tables) to estimate the capacitance of net connections. --

Please replace the paragraph beginning at page 13, line 11 with the following rewritten paragraph:

--However, the invention takes advantage of the parasitic capacitance C of the redistribution metal to control the signal slew rate. By calculating the amount of capacitance needed to achieve an RC time constant corresponding to a desired slew rate using the known driver output impedance Z_D ~~resistance R_O~~, the length of the redistribution metal is chosen to leverage the parasitic capacitance C of the chosen redistribution metal to essentially "program" the slew rate of the signal on the transmission line. The added advantage of the inventive technique for controlling the slew rate of signals is that it requires no slew rate control circuitry which would otherwise add complexity and cost to the chip.--